1. A method for forming a calibrated critical dimension test wafer for process control of sub-tenth micron polysilicon features comprising:

(a) providing a wafer substrate;

(b) forming a pad oxide on said wafer substrate;

(c) depositing a metal layer on said pad oxide;

(d) patterning said metal layer to form at least one metal plate in at least one region of said wafer substrate;

(e) milling a plurality of substantially parallel trenches in said at least one metal plate with a focused ion beam, thereby forming a critical dimension test array; and

(f) measuring the widths of said parallel trenches and the spacings therebetween, thereby calibrating said critical dimension test array.

2. The method of claim 1 wherein said pad oxide is silicon oxide thermally grown to a thickness of between about 50 and 200 nm.

3. The method of claim 1 wherein said metal layer is between about 400 and 1,000 nm. thick.

4. The method of claim 1 wherein said metal layer is an alloy of aluminum and copper wherein the copper content is between about 0.1 and 1.0 percent by weight.

5. The method of claim 1 wherein said ions are germanium.

6. The method of claim 1 wherein said ion beam has an energy of between about 25 and 35 keV and a current of between about 0.5 and 3 pA.

7. The method of claim 1 wherein said trenches are between about 30 and 90 nm. wide and have a width uniformity 3-sigma of between about 3.0 and 3.5 nm.

8. The method of claim 1 wherein said trenches have a mean value of width roughness of between about 3.0 and 3.7nm. and a mean value of edge roughness of between about 1.8 and 2.2 nm.

9. The method of claim 1 wherein said measuring is accomplished using a calibrated scanning electron microscope.

10. A method for using a calibrated critical dimension test wafer for process control of sub-tenth micron polysilicon features in an integrated circuit process comprising:

(a) providing a calibrated critical dimension test wafer having a plurality of substantially parallel trenches milled, with a focused ion beam, in a metal plate formed over a pad oxide, and calibrated according to the process cited by Claim 1;

(b) mounting and inserting said calibrated critical dimension test wafer in the sample chamber of a process control scanning electron microscope;

(c) calibrating said process control scanning electron microscope by measuring the widths of said trenches and the spaces therebetween; and

(d) after said calibrating, using said process control scanning electron microscope to measure widths and spacings of polysilicon lines on an in-process integrated circuit wafer.

11. The method of claim 10 wherein said pad oxide is silicon oxide thermally grown to a thickness of between about 50 and 200 nm.

12. The method of claim 10 wherein said metal plate is between about 400 and 1,000 nm. thick.

13. The method of claim 10 wherein said metal plate is an alloy of aluminum and copper wherein the copper content is between about 0.1 and 1.0 percent by weight.

14. The method of claim 10 wherein said focused ion beam comprises germanium ions.

15. The method of claim 10 wherein said focused ion beam has an energy of between about 25 and 35 keV and a current of between about 0.5 and 3 pA.